54AC/74AC258 • 54ACT/74ACT258

Quad 2-Input Multiplexer With 3-State Outputs

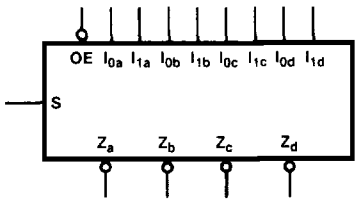
Description

The 'AC/'ACT258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented sytems.

- **Multiplexer Expansion by Tying Outputs Together**
- **Inverting 3-State Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT258 has TTL-Compatible Inputs**

Ordering Code: See Section 6

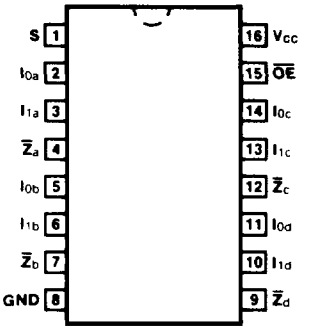
Logic Symbol



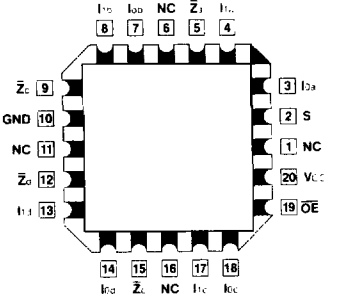
Pin Names

S	Common Data Select Input
$\overline{OE}$	3-State Output Enable Input
I_{0a} - I_{0d}	Data Inputs from Source 0
I_{1a} - I_{1d}	Data Inputs from Source 1
$\overline{Z}_a$ - $\overline{Z}_d$	3-State Inverting Data Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

Functional Description

The 'AC/'ACT258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'AC/'ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$\overline{Z}_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z}_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$\overline{Z}_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

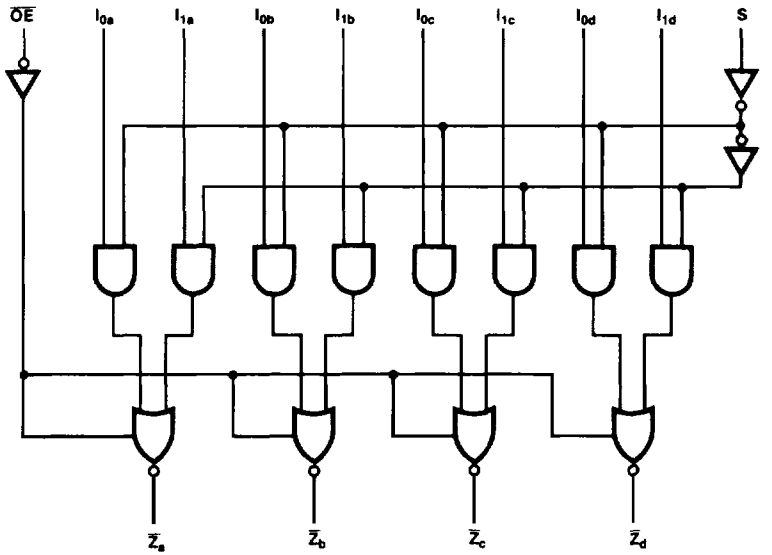
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT258)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0	1.0 1.0	6.0 4.5	9.5 7.5	1.0 1.0	12.0 9.5	1.0 1.0	11.0 8.5	ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0	1.0 1.0	5.0 4.0	8.5 6.5	1.0 1.0	10.5 7.5	1.0 1.0	9.5 7.0	ns	3-5
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3 5.0	1.0 1.0	7.5 6.0	12.0 9.5	1.0 1.0	15.0 12.0	1.0 1.0	14.0 10.5	ns	3-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3 5.0	1.0 1.0	7.5 5.5	11.5 9.0	1.0 1.0	14.0 10.5	1.0 1.0	13.0 10.0	ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	6.0 4.5	9.5 7.5	1.0 1.0	11.5 9.0	1.0 1.0	10.5 8.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	5.5 5.5	9.0 7.0	1.0 1.0	10.5 8.5	1.0 1.0	10.0 8.0	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.5 5.5	10.0 8.5	1.0 1.0	11.5 9.5	1.0 1.0	11.5 9.0	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.5 5.0	9.0 7.0	1.0 1.0	10.5 8.5	1.0 1.0	10.0 8.0	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	6.5	8.5			1.0	9.5	ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	5.5	7.5			1.0	8.0	ns	3-5
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	7.5	10.5			1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	7.0	9.5			1.0	11.0	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	6.5	8.5			1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	6.5	8.5			1.0	9.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	9.0			1.0	10.0	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	6.0	8.0			1.0	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	55.0	pF	$V_{CC} = 5.5$ V